**INTEL UNNATI PROGRAM 2023**

**SAIRAM GROUP OF INSTITUTIONS**

**DESIGN AND IMPLEMENTATION OF ATM CONTROLLER USING FSM**

**Submitted by**

**DEEPTTHA SRI S**

Team name: PEONY

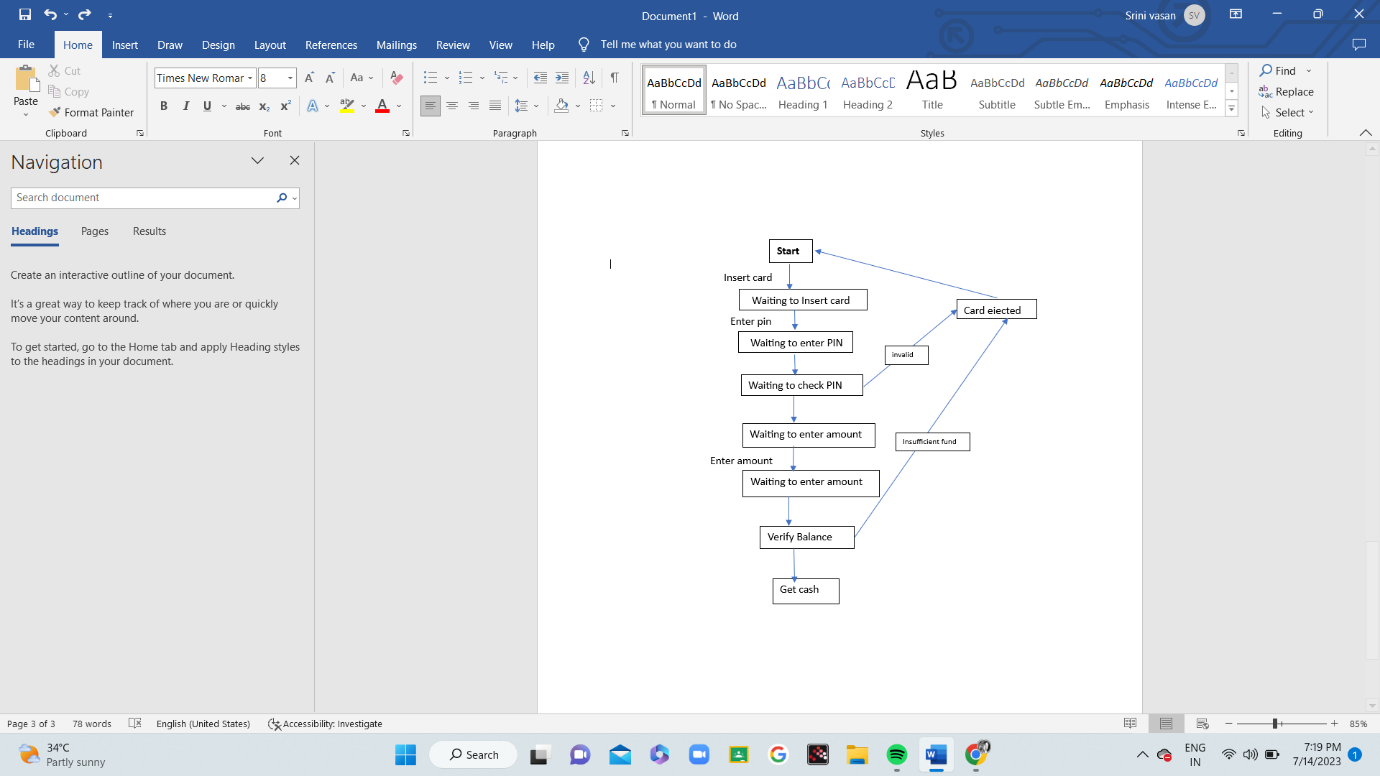
Internal mentor: Dr. Priya S

Industrial mentor: Mr. Abhishek

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BLOCK DIAGRAM



FSM MODEL

An FSM (Finite State Machine) is a mathematical model used to design and digital

logic circuits. It is conceived as an abstract machine that can be in one of a finite

number of states. The machine is in only one state at a time; the state it is in at any

given time is called the current state. It can change from one state to another when

initiated by a triggering event or condition, this is called a transition. A particular

FSM is defined by a list of the possible transition states from each current state, and

the triggering condition for each transition.

A finite state machine is an abstract model describing the synchronous sequential

machine. Before going for the design of sequential machines one should be

familiar with the following things.

In synchronous or clocked sequential circuits, clocked flip-flops are used as

memory elements, which change their individual states in synchronism with the

periodic clock signal. Therefore the change in state of the entire circuit occurs at

the transition of the clock signal.

The synchronous or clocked sequential are represented by two models

(1) Mealy state machine.

(2) Moore state machine.

Mealy State Machine

In this model the output depends on both the present state of the flipflop(s) and the input(s).

The use of a Mealy FSM leads often to a reduction of the numberof states.

Mealy FSM is difficult to design.

One disadvantage in mealy is as output is dependent on input, even a small glitch in input is seen in the output.

Moore State Machine

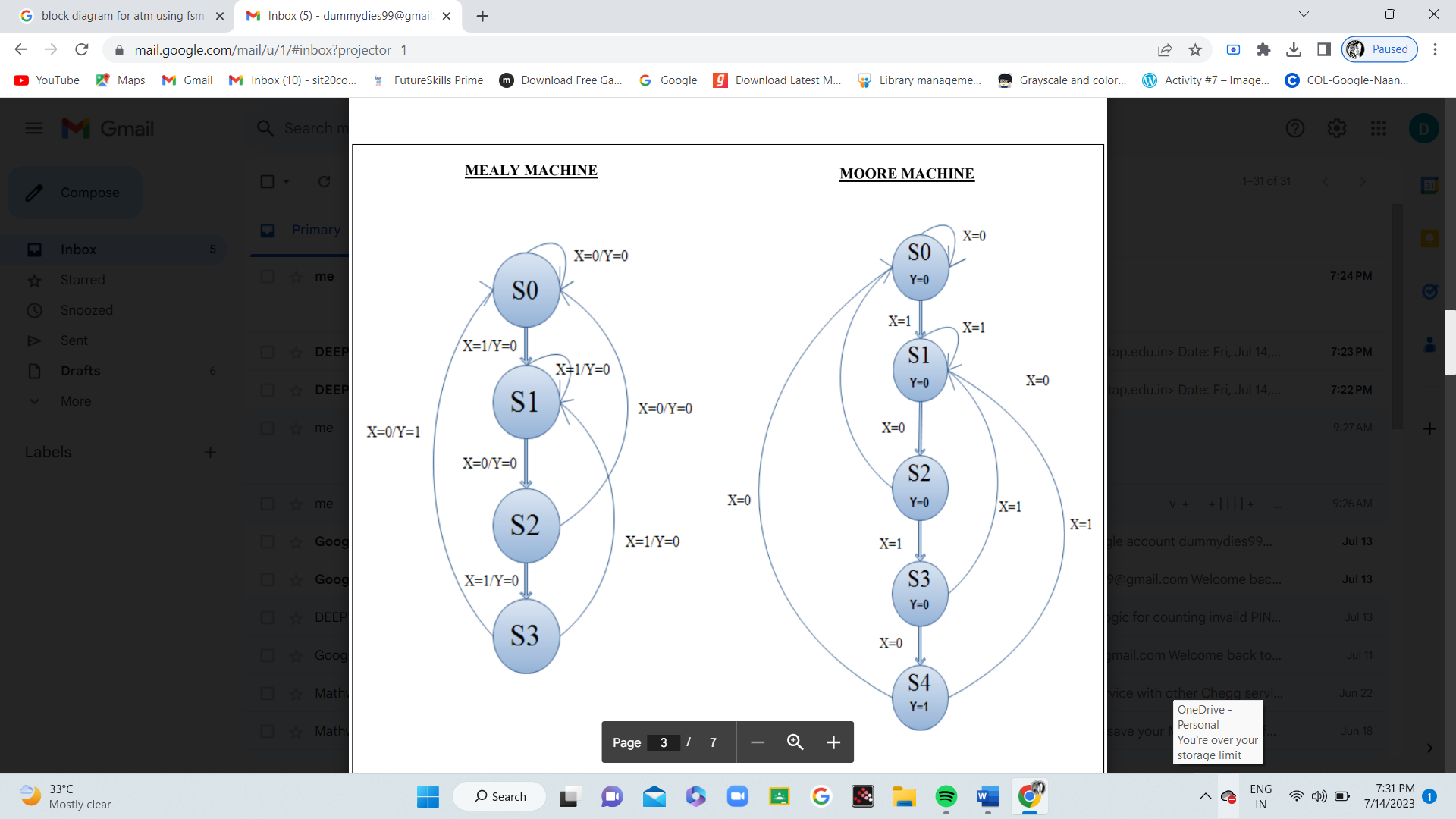
In this model output depends only on the present state of the flipflops.

In Moore FSM the number of states compared to mealy FSM will be increased by one or more.

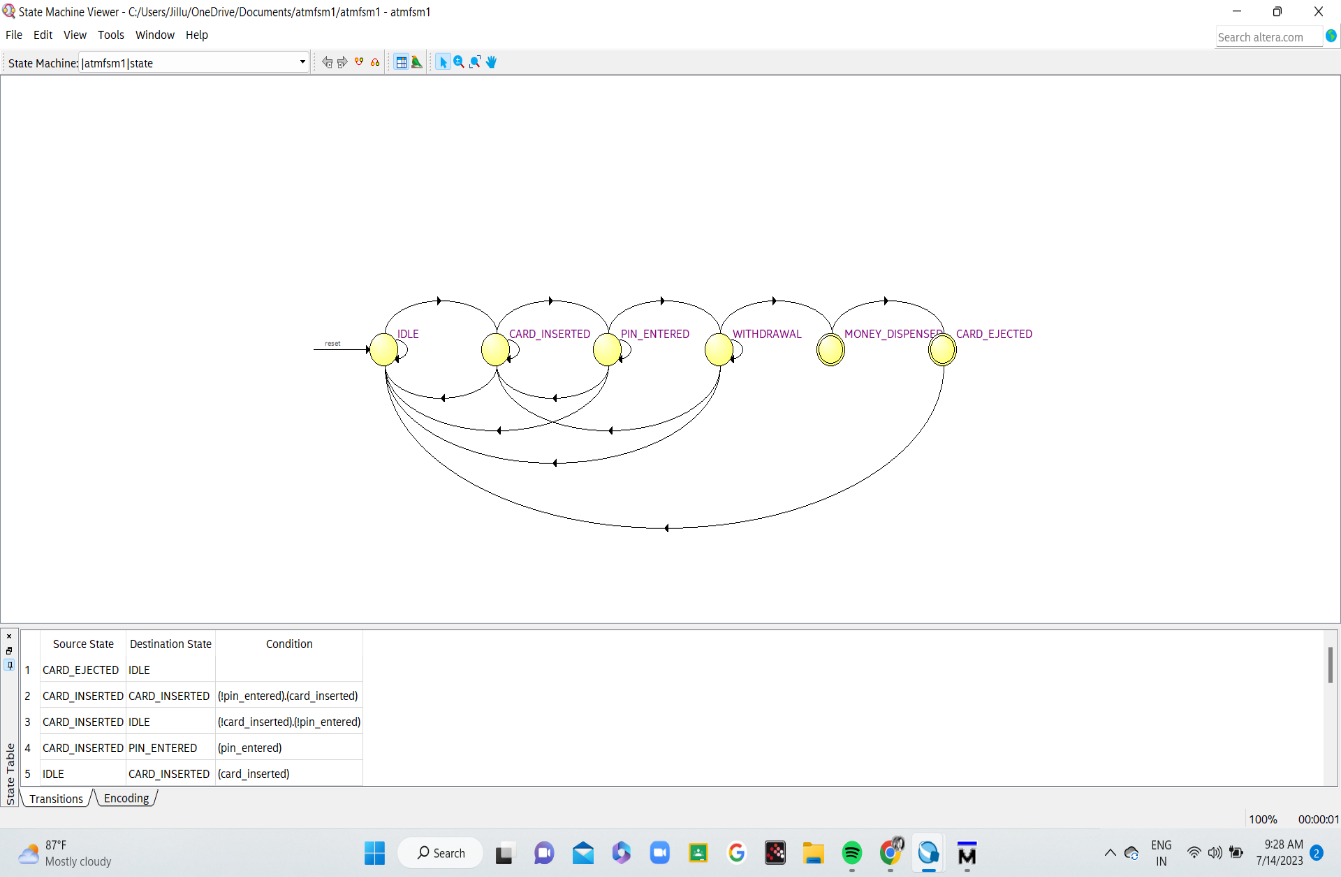
Moore FSM is easy to design and analyze compared to mealy.

Moore model is glitch free as it is dependent only on the present state.

CHOSEN MODEL FOR DESIGNING ATM



STATE DIAGRAM – ATM CONTROLLER USING MEALEY STATE



This project is implemented using Mealey state machine and the above diagram explains the approach towards the interaction between the states

This Mealy state diagram provides a visual representation of the state transitions and the associated output signals in the ATM system, as implemented in the Verilog HDL code using a Mealy state machine.

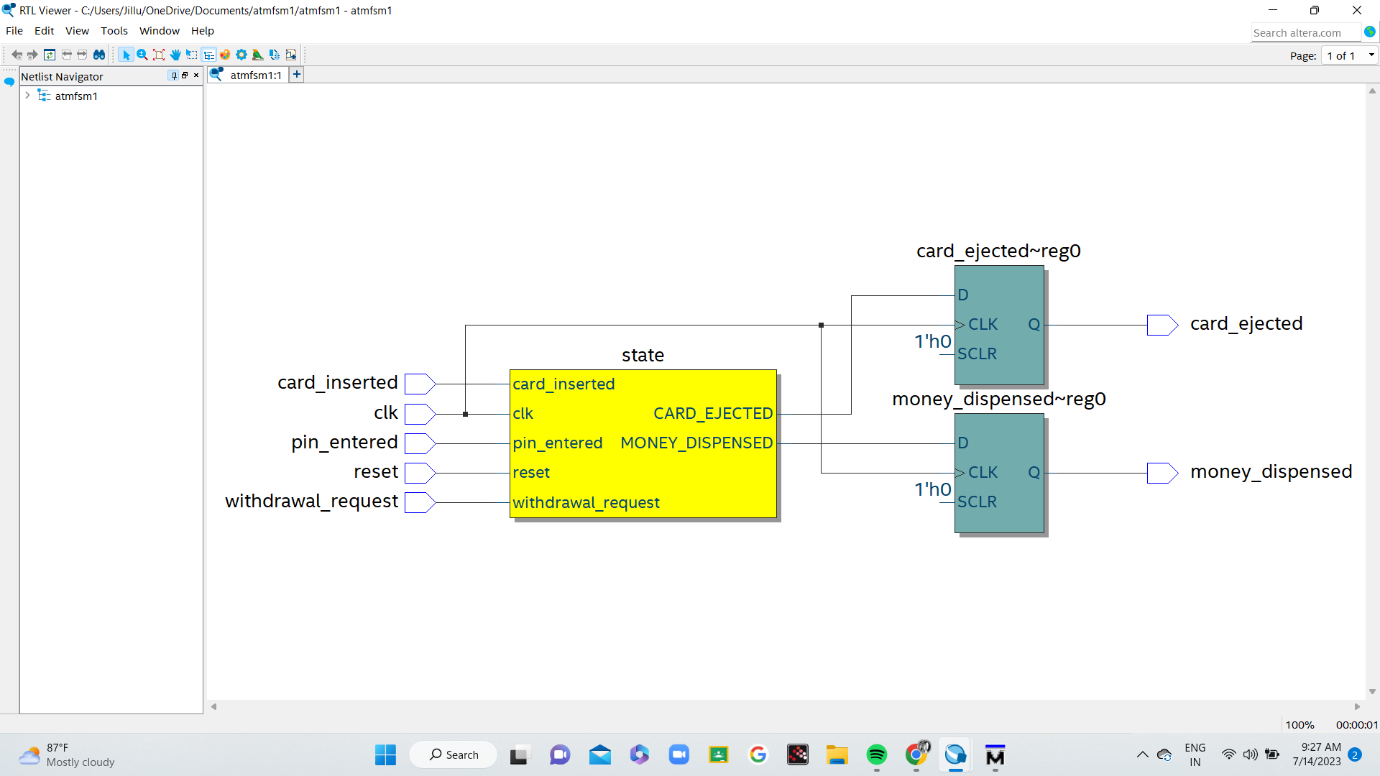
The Mealy model is characterized by having outputs that depend not only on the current state but also on the inputs. In this case, the money\_dispensed output is based on the transition from the WITHDRAWAL state to the MONEY\_DISPENSED state, and the card\_ejected output is based on the transition from the MONEY\_DISPENSED state to the CARD\_EJECTED state.

DEMONSTRATION

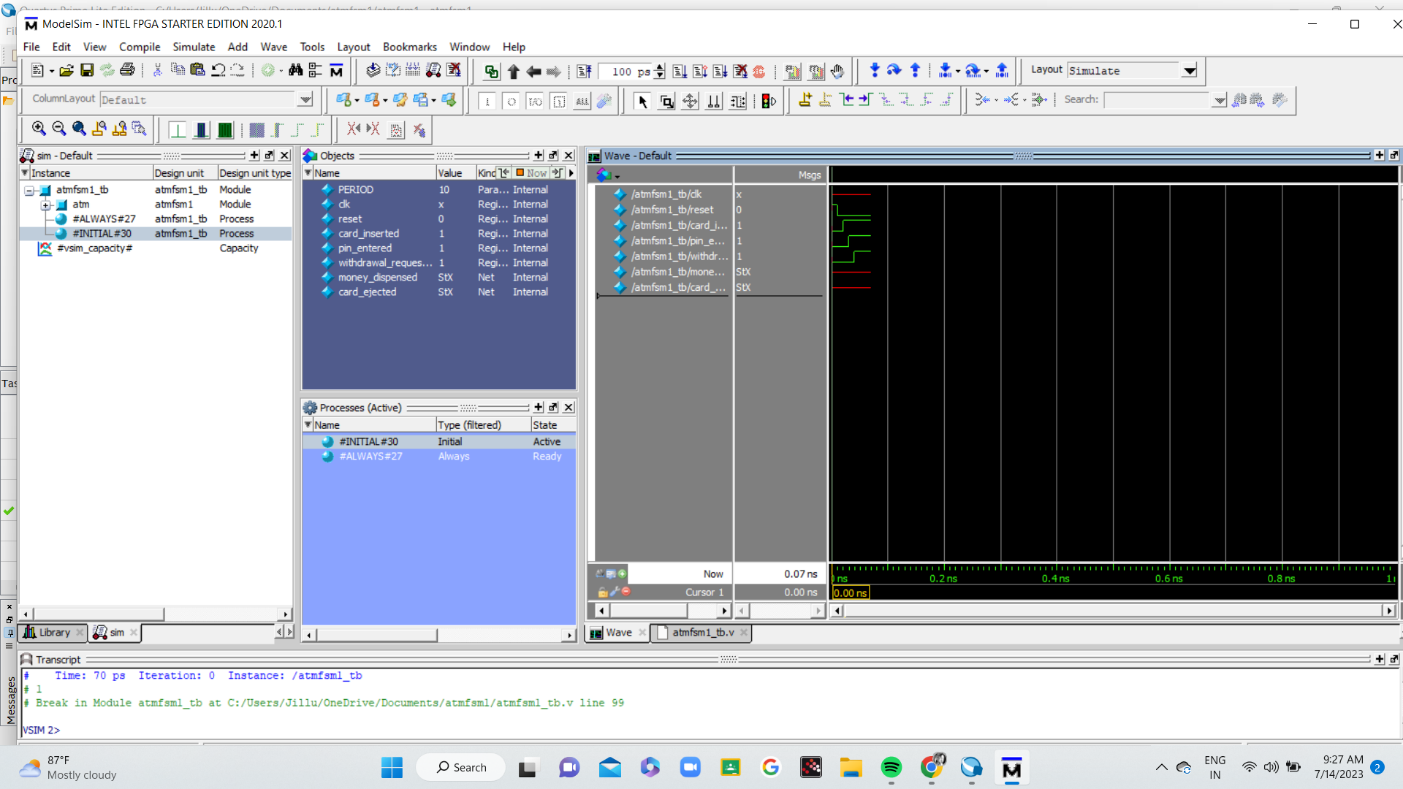


SCREENSHOTS

1. RTL VIEW



2.RTL SIMULATION - MODEL SIM

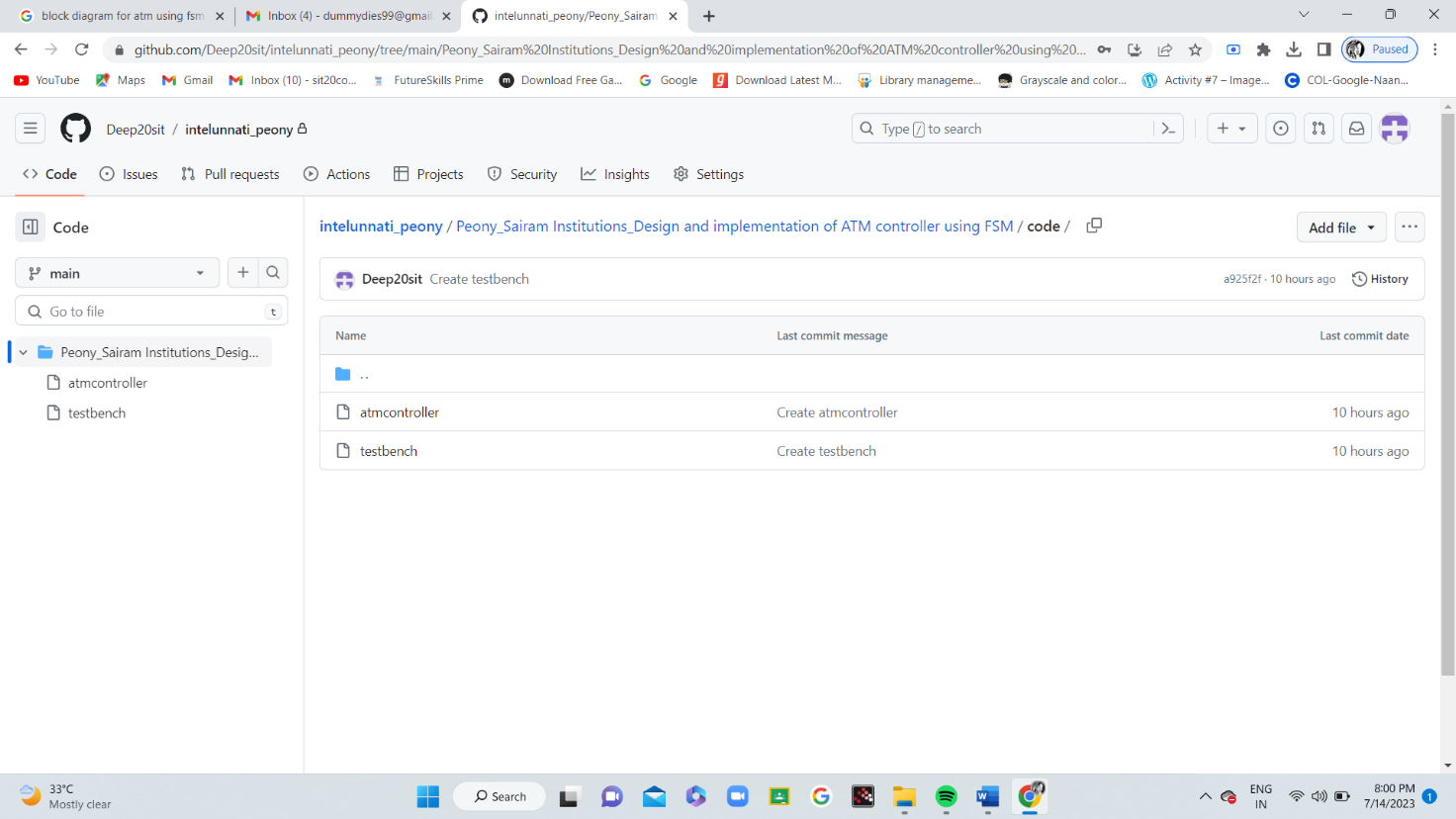


GIT HUB REPOSITORY

LINK

https://github.com/Deep20sit/intelunnati\_peony

SCREENSHOTS



CONCLUSION

An ATM controller is designed using Mealey state model using Intel Quartus lite software and the EDA tool to run the simulation is Modelsim altera. This project is useful to understand the Finite state machine and FPGA implementation. This can be enhanced by adding face recognition and try using moore state machine for designing.